REMARKS

In the Office Action, the Examiner indicated that claims 1 through 38 are pending in the application and the Examiner rejected claims 1-6, 9-23, 25-30, and 33-38.

Claim Rejections, 35 U.S.C. §103

On page 3 of the Office Action, the Examiner rejected claims 1-6, 9-19, 21-23, 25-30, and 33-37 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,212,263 to Sun et al. in view of U.S. Patent No. 6,137,392 to Herbert and further in view of U.S. Patent No. 6,553,216 to Pugel et al.

On page 7 of the Office Action, the Examiner rejected claim 38 under 35 U.S.C. §103(a) as being unpatentable over Sun et al. in view of Herbert and further in view of U.S. Patent No. 5,311,086 to Yamaji et al.

On page 8 of the Office Action, the Examiner rejected claim 20 under 35 U.S.C. §103(a) as being unpatentable over Sun et al. in view of Herbert and further in view of Pugel et al., and further in view of U.S. Patent No. 6,169,762 to Embree et al.

The Present Invention

This invention improves the attenuation of an undesired signal found in a differential signal path by using inductive, as opposed to capacitive, coupling. The inventive electrical interface includes a primary inductor, a secondary inductor, and a filter. The primary inductor and the secondary inductor operably couple an input differential signal pair to an

output differential signal pair, and the filter attenuates an undesired signal in the output differential signal pair. The input differential pair is formed by using a differential driver, e.g., a CODEC, to generate the pair from a single input line (e.g., a tip line).

The invention includes a parasitic capacitor operably coupled between the primary and the secondary inductor. The parasitic capacitor has a capacitance that is as small as possible while still preventing common mode noise signals from interfering with signals being transmitted over the input differential pair. In a preferred embodiment, the capacitance is in the range of approximately 0.5 pF to approximately 2.5 pF.

The invention also includes a method for interfacing an input differential signal pair to an output differential signal pair. In particular, the method includes the steps of inductively coupling the input differential signal pair to an output differential signal pair, and filtering out a common mode signal occurring in the output differential signal pair. The inventive method improves the attenuation of an undesired signal found in a differential signal path by using inductive coupling.

U.S. Patent No. 6,212,263 to Sun et al.

U.S. Patent No. 6,212,263 to Sun et al. ("Sun") teaches a combination X digital subscriber line (xDSL) and analog modem that includes a computer bus interface, CODECs, an analog front end for xDSL communications coupled to a POTS line and a direct access arrangement for analog communication also connected to the POTS line. Sun is teaching the transfer of ADSL data in the 10 kHz to 1 MHz band also referred to as "base band". These

base band signals are those signals defined in the ADSL standard E1-T1 413 issue 2 and its successors. ADSL data by its nature is high entropy data, that is, it contains large amounts of information in each symbol. As is well known, there are clear differences in the characteristics of low frequency, high entropy data such as ADSL data and high frequency, low entropy data. The Examiner acknowledges that Sun fails to teach a capacitor operably coupled between a primary inductor and a secondary inductor.

U.S. Patent No. 6,137,392 to Herbert ("Herbert")

U.S. Patent No. 6,137,392 to Herbert ("Herbert") teaches a transformer for switched power mode power supplies comprising an input stage transformer. This transformer is designed for improved coupling and low primary leakage inductance, without regard for insulation above "working insulation" or for interwinding capacitance. One or more additional stage transformer sections are optimized for low interwinding capacitance and high dielectric isolation. The secondary of the input stage device drives the primary of the next stage, so that the transformer stages are in series. Accordingly, the total interwinding capacitance from end to end is low and the total dielectric isolation from end to end is high. The secondary of the input stage transformer is isolated from both the input and the output, so it can be grounded as a safety measure (Herbert, abstract and summary). The Examiner relies on Herbert for an alleged teaching of a capacitor operably coupled between a primary inductor and a secondary inductor, however the Examiner acknowledges that Herbert fails to teach a

parasitic capacitor with a capacitance value in a range of approximately 0.5 pF to approximately 2.5 pF.

U.S. Patent No. 6,553,216 to Pugel et al. ("Pugel")

U.S. Patent No. 6,553,216 to Pugel et al. ("Pugel") teaches a tuner for a tunable filter used in selecting a desired RF signal in response to a tuning control signal. Pugel also teaches a tunable image trap for rejecting the undesired image signal corresponding to the desired RF signal responsive to the tuning control signal coupled in cascade between an RF amplifier and a mixer. The tunable trap serves as an impedance transformation element between the tunable filter and the mixer. This arrangement is particularly useful in a tuner in which the frequency range of the local oscillator signal is below the frequency range of the received RF signals (Pugel, abstract and summary). The Examiner relies on Pugel for an alleged teaching of a parasitic capacitor with a capacitance value in a range of approximately 0.5 pF to approximately 2.5 pF.

U.S. Patent No. 5,311,086 to Yamaji et al. ("Yamaji")

U.S. Patent No. 5,311,086 to Yamaji et al. ("Yamaji") teaches a multiplying circuit in which a pair of common-base transistors each having a small emitter area are inserted between the common emitter terminals of the first and second differential amplifiers. The output of the differential amplifiers are connected to the inputs of a second set of differential amplifiers. The second set of differential amplifiers provides the input for a third set and the pattern

continues until a predetermined DC offset characteristic is achieved, resulting in a multiplier circuit (Yamaji, abstract and summary). The Examiner relies on Yamaji for an alleged teaching of the parasitic capacitor having a capacitance that is as small as possible while still preventing common mode noise signals from being transmitted over said input differential pair.

U.S. Patent No. 6,169,762 to Embree et al. ("Embree")

U.S. Patent No. 6,169,762 to Embree et al. ("Embree"), assigned to Lucent Technologies, Inc., teaches interface devices that provide an interface between a first device and a second device, where the interface device provides electrical isolation between the first device and the second device, and where CODEC processing is distributed between the first-device side and the second-device side of the interface device. The Examiner relies on Embree et al. for the teaching of a shunt regulator for the purpose of protecting the line-side device, making specific reference to Figure 3, shunt regular 312 of Embree. Applicant notes herein that Embree et al. is not prior art, since at the time the present invention was made, it too was assigned to Lucent Technologies, Inc., as set forth in the previously submitted "Microelectronics Patent Committee Invention Submission," dated June 5, 2000, which clearly indicates it as being proprietary information of Lucent Technologies, Inc. Since the subject matter of Embree, which qualifies as prior art only under 35 U.S.C. §102(e), and the claimed invention were, at the time the invention was made, owned by the same person or

subject to an obligation of assignment to the same person, Embree is not prior art pursuant to 35 U.S.C. §103(c).

The Examiner has not Established a *prima facie* Case of Obviousness

As set forth in the MPEP:

> To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings.
> MPEP 2143

Applicant has previously amended and/or added to the independent claims to focus the present invention on the use of a parasitic capacitor between the primary inductor and the secondary inductor, and using a capacitance value for the parasitic capacitor that is as small as possible while still preventing common mode noise signals from interfering with signals being transmitted over the input differential pair. In a preferred embodiment, this capacitance value is in a range of approximately 0.5 pF to approximately 2.5 pF.

Since the Examiner has acknowledged that Sun fails to teach a capacitance operably coupled between the primary inductor and the secondary inductor, the focus of this argument turns to the Examiner's assertion that Herbert teaches a capacitor coupled between the primary and secondary inductors for the purpose of obtaining a high dielectric isolation, and the Examiner's assertion that Pugel teaches a filter capacitor in the range of approximately 0.5 to approximately 2.5 pF.

The Examiner looks to Herbert to teach a capacitance operably coupled between the primary inductor and the secondary inductor and provide motivation for including this as an added feature to the system provided by Sun. The Examiner says it would be obvious to modify the transformer taught by Sun (shown in Sun, Fig. 6) to include a parasitic capacitor operalby coupled between the primary inductor and the secondary inductor as taught by Herbert. However, no motivation is provided by the Examiner for specifically adding the parasitic capacitor. The Examiner states the result would be a high dielectric isolation, but this result is the end result of the complete system disclosed by Herbert, by linking several transformers. This result is not directly related to the addition of the parasitic capacitor to one transformer. Additionally, the Examiner provides neither a reference in Sun stating it would be beneficial to have a high dielectric isolation nor a reference in Herbert stating it would be beneficial to utilize a parasitic capacitor in a power supply circuit as taught by Sun. At best, impermissible hindsight is being used to attempt to find a basis for rejecting the claimed invention under 35 U.S.C. §103. However, since fundamental teachings and/or suggestions, which would be required to make the rejections valid, are missing, the rejection of the claims must fail.

Secondly, the Examiner looks to Pugel to teach the capacitor has a capacitance in the range of approximately 0.5 pF to approximately 2.5 pF. Pugel is directed towards a tuner for filtering RF signals which utilizes a 2 pF capacitor in the disclosed circuitry. However, Pugel provides no motivation for using a 2pF capacitor in either the power supply circuit of Sun or the switched mode transformer of Herbert. Additionally, the Examiner provides no

motivation in the rejection from Pugel to modify either Sun or Herbert. Herbert teaches a system operating on a power scale that exceeds the power scale of the present invention by a factor of greater than 1000. Nowhere does Herbert suggest utilizing low capacitance components, such as the presently claimed parasitic capacitor. At best, impermissible hindsight is being used to attempt to find a basis for rejecting the claimed invention under 35 U.S.C. §103. However, since fundamental teachings and/or suggestions, which would be required to make the rejections valid, are missing, the rejection of the claims must fail.

With regard to claim 38, similar arguments as stated above apply. No motivation is provided to combine Sun and Herbert. Additionally, the Examiner looks to Yamaji to teach the parasitic capacitor has a capacitance that is as small as possible while still preventing common mode noise signals being transmitted over said input differential pair. However, the portion of Yamaji cited by the Examiner contradicts this assertion. In particular, the Examiner cites col 3 lines 7-14, which states:

> "The CMRR of the differential amplifier decreases in a high frequency range (radio frequency band) due to an increase in the parasitic capacitance of transistors in use and the degree of one input signal leaking from one input terminal pair to the other input terminal pair increases."

Several other passages of Yamaji suggest maintaining a large parasitic capacitance, the first occasion at col 4 lines 34-41.

In addition to Yamaji not teaching or reasonably suggesting the claimed limitation, the Examiner provides no motivation from Yamaji to modify either Sun or Herbert. Herbert teaches a system operating on a power scale that exceeds the power scale of the present

invention by a factor of greater than 1000. Nowhere does Herbert suggest utilizing low capacitance components, such as the presently claimed parasitic capacitor. At best, impermissible hindsight is being used to attempt to find a basis for rejecting the claimed invention under 35 U.S.C. §103. However, since fundamental teachings and/or suggestions, which would be required to make the rejections valid, are missing, the rejection of the claims must fail.

With regard to the rejection of claim 20 as being unpatentable over Sun in view of Herbert, and further in view of Pugel, and further in view of Embree, applicant notes that Embree is not prior art, since at the time the present invention was made, it too was assigned to Lucent Technologies. Since the subject matter of Embree, which qualifies as prior art only under 35 U.S.C. §102(e), and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person, Embree is not prior art pursuant to 35 U.S.C. §103(c). Therefore, the Examiner is respectfully requested to reconsider and withdraw the 103(a) rejection to claim 20.

For these reasons, the claimed invention patentably defines over the cited references and is in allowable condition.

To even more clearly point out the differences between the claimed invention and the cited references, applicant notes that the minimization of the capacitance between the primary and secondary is a key element of the present invention. With inductive coupling, there is always some amount of common mode voltage that is present, and the common mode voltage exists over a wide band of frequencies. That very wide band of frequencies can interfere with

circuits connected to capacitively coupled circuits and cause the circuits to fail, due to the interference. Sun, in teaching the transfer of base band signals, transfers signals in the frequency range between 100 Hz and 4 kHz. By contrast, the present invention is a pass band signaling scheme and will be transmitting signals in the MHz range. Further, as noted above, Sun is an ADSL systems, which use high entropy data. With high entropy data, the filtering boundaries must be very clearly defined. For example, with ADSL, the filters must have a very clearly-defined pass band, transition band, and stop band. By contrast, the low entropy data being transmitted with the present invention does not require this level of precision and thus can have, for example, low pass filtering and high pass filtering that together attenuates signals over a wide frequency range of approximately 50 kHz to approximately 10 MHz.

Since each of the independent claims specifically recite the minimization of the capacitance of the parasitic capacitor (claims 1, 21, and 30 specifying the range of 0.5 pF to 2.5 pF and claim 38 specifying that the capacitance be minimized according to certain parameters), the claimed invention patentably defines over the prior art.

Conclusion

The present invention is not taught or suggested by the prior art. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the rejection of the claims. An early Notice of Allowance is earnestly solicited.

Enclosed herewith, in duplicate, is a Petition for extension of time to respond to the Examiner's Action, and a Credit Card Payment Form authorizing the payment of the extension

fee. The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 19-5425.

Respectfully submitted

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Date

Mark D. Simpson, Esquire
Registration No. 32,942

SYNNESTVEDT & LECHNER LLP
2600 ARAMARK Tower
1101 Market Street
Philadelphia, PA 19107
Telephone: (215) 923-4466
Facsimile: (215) 923-2189

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